REMARKS

In response to the above-identified Final Office Action, Applicant amends the application and seeks reconsideration thereof. In this response, Applicant amends claims 8 and 15, and cancels claims 12 and 19. Applicant does not add any new claims. Accordingly, claims 8-10, 13-17 and 20-21 are pending.

I. Claims Rejected Under 35 U.S.C. §103(a)

The Patent Office rejects claims 8-10, 14-17 and 21 under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 4,015,281 issued to Nagata et al. ("Nagata") in view of U.S. Patent No. 5,990,516 issued to Momose et al. ("Momose"). Applicant amends claims 8 and 15.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. See MPEP § 2143; see also <u>In re Ray Baeck</u>, 947 F.2d 488; 20 USPQ 2d 1438 (Fed. Cir. 1991).

Regarding claim 8, among other elements, amended claim 8 includes a transistor device comprising a first dielectric material selected from one of HfO₂, BaO, La₂O₃, Y₂O₃, and ZrO₂ and having a first dielectric constant. As noted in the Application, these dielectric materials each have a heat of formation greater than a heat formation of SiO₂. See <u>Application</u>, page 8, lines 19-21. The greater heat of formation tends to limit the defect interface. See <u>Application</u>, page 8, lines 21-23.

In making the rejection, the Patent Office characterizes Nagata as teaching each of the elements of claim 8 except a set of feature size technologies defined by a gate length in the range of

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25-125 nm. See <u>Paper No. 25</u>, page 2. The Patent Office relies in <u>Momose</u> to cure the defects of <u>Nagata</u>.

The Patent Office characterizes <u>Momose</u> as showing a semiconductor device having double layer gate dielectric in which the feature size technology has a gate length of 150 nm (or 0.15 mm) to form a high performance semiconductor having low power consumption. See <u>Paper No. 25</u>, page-3-(citing-<u>Momose</u>, col.-16, lines 28-48 and col.-16, line 66 through col. 17, line 32). The Patent Office further characterizes <u>Momose</u> as showing that the gate length can be decreased even more to improve the current drive capability and in one embodiment had a length of 40 nm. See <u>Paper No. 25</u>, page 3 (citing <u>Momose</u>, col. 15, lines 13-31).

Nagata teaches, "an enhancement type and a depletion type metal-insulator-semiconductor field effect transistor being formed on a common substrate of silicon and electrically isolated from each other by a plurality of layers including, for example, a first layer of SiO₂, a second layer of Al₂O₃ capable of inducing holes in the surface portion of the substrate, and a third layer of SiO₂, and the relation between the thickness of these layers is suitably selected for attaining satisfactory isolation between these transistors." See Nagata, Abstract. Therefore, Nagata teaches field effect transistors having layers of only SiO₂ and Al₂O₃. Nagata does not describe Al₂O₃ as having a heat of formation greater than SiO₂ so as to produce a reduced defect interface. In addition, Nagata does not teach or suggest a transistor device comprising a first dielectric material selected from one of HfO₂, BaO, La₂O₃, Y₂O₃, and ZrO₂. Thus, Nagata fails to teach or suggest each of the elements of claim 8.

As mentioned above, the Patent Office relies on Momose to cure the defects of Nagata.

Momose teaches a semiconductor device comprising a P-type semiconductor substrate having an insulating film, a gate electrode formed on the substrate via the insulating film, and an N-type source/drain region formed on both sides of a channel forming region located under the gate electrode formed on the substrate. Momose, Abstract. Momose discloses the layers are comprised of silicon oxide, silicon nitride, silicon nitric oxide, stacks of silicon nitride and silicon oxide, and laminated layers of tantalum oxide, titanium oxide, strontium and its silicon oxide or silicon nitride

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films. See <u>Momose</u>, col. 16, line 66 - col. 17, line 11. Therefore, <u>Momose</u> fails to teach or suggest a transistor device comprising a first dielectric material selected from one of HfO_2 , BaO, La_2O_3 , Y_2O_3 , and ZrO_2 . Thus, <u>Momose</u> fails to cure the defects of <u>Nagata</u>.

The failure of <u>Momose</u> to cure the defects of <u>Nagata</u> is fatal to the obviousness rejection.

Therefore, claim 8 is not obvious over <u>Nagata</u> in view of <u>Momose</u>. Accordingly, Applicant respectfully-requests-withdrawal-of the-rejection-of independent-claim-8.

Claims 9-10 and 13-14 each depend from claim 8 and contain all of the limitations thereof. Therefore, claims 9-10 and 13-14 are not obvious at least for the same reasons as claim 8.

Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 9-10 and 13-14.

Regarding the rejection of claim 15, among other elements, claim 15 includes a first dielectric material selected from one of HfO_2 , BaO, La_2O_3 , Y_2O_3 , and ZrO_2 similar to claim 8. Therefore, the discussion above regarding the combination of Nagata and Momose failing to teach or suggest a first dielectric material selected from one of HfO_2 , BaO, La_2O_3 , Y_2O_3 , and ZrO_2 is equally applicable to a similar limitation defined in claim 15. Therefore, claim 15 is not obvious over Nagata in view of Momose. Accordingly, Applicant respectfully request withdrawal of the rejection of claim 15.

Claims 16-17 and 20-21 depend from claim 15 and contain all of the limitations thereof. Therefore, claims 16-17 and 20-21 are not obvious over <u>Nagata</u> in view of <u>Momose</u> at least for the same reasons as claim 15. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 16-17 and 20-21.

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CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Patent Office believes that a telephone conference would be useful in moving the application forward to allowance, the Patent Office is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated:

12400 Wilshire Boulevard Seventh Floor Los Angeles, California 90025 (310) 207-3800 CERTIFICATE OF MAILING:

William Thomas Babbitt; Reg. No. 39,591

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on _/6/69.

Nadva Gordon

Date